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APPLICATION N	O. F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/762,788		01/22/2004	Samir Chaudhry	CHAUDHRY	CHAUDHRY 6125	
47396	7590	03/21/2005		EXAMINER		
	AINES, PC		PHAM, LONG			
	AGERE SYSTEMS INC. PO BOX 832570				PAPER NUMBER	
RICHARI	OSON, TX	75083	2814			

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



	Application No.	Applicant(s)				
	10/762,788	CHAUDHRY ET AL.				
Office Action Summary	Examiner	Art Unit				
	Long Pham	2814				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on						
•	action is non-final.					
,	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) Claim(s) 23-40 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 23-40 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examine	er.					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)	» — · · · · ·	(DTO 442)				
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>01/22/04</u>. 	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Holloway et al. (US patent 4,845,047).

With respect to claim 23, Holloway et al. teach a process for fabricating an integrated circuit, comprising (see fig. 1 and col. 6, lines 45-55):

forming a gate structure over a substrate, said gate structure having a length of approximately 1.25 micrometer; and

forming a source and drain, said source and said drain not having lightly doped regions.

With respect to claim 25, Holloway et al. further teach forming an oxide layer over the substrate and a conductive layer over the oxide layer.

3. Claim 33 is rejected under 35 U.S.C. 102(b) as being anticipated by Holloway et al. (US patent 4,845,047).

With respect to claim 33, Holloway et al. teach a process for fabricating an integrated circuit, comprising (see fig. 1 and col. 6, lines 45-55):

forming an oxide layer over a substrate;

forming a conductive layer over said oxide layer, said oxide layer and said conductive layer forming a gate having a length of 1.25 micrometer; forming a channel in said substrate; and

forming a source and a drain, said source and said drain not having lightly doped regions.

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Claim Rejections - 35 USC § 103

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24, 26, 27, 28, 29, 30, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway et al. (US patent 4,845,047) as applied to claims 23 and 25 above, and further in view of Adan (US patent 6,288,425) and Ueno et al. (US patent 6,815,295).

With respect to claim 24, Holloway et al. fail to teach that the channel is formed before the source and drain are formed.

Adan teaches a process in which channel region is formed before source and drain are formed. See col. 2, lines 50-65.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to incorporate Adan's above teaching into the process of Holloway et al. to improve manufacturing yield. See col. 8, lines 40-45.

With respect to claim 26, Holloway et al. fail to teach that the channel is doped by a halo implantation.

However, doping channel by halo implantation is well-known in the art.

With respect to claim 27, Holloway et al. fail to teach that the gate length is in the range between .05 to .25 micrometer.

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However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to reduce the length of gate because it is known that shorter gate length would achieve device scaling.

With respect to claim 28, Holloway et al. fail to teach gate oxide comprises of a first oxide layer and a second oxide layer.

Ueno et al. teach a process in which a gate oxide comprises of a first oxide layer and a second oxide layer. See col. 28, lines 15-25.

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to form gate oxide made from a first oxide layer and a second oxide layer to reduce the processing steps. See col. 28, line 38.

With respect to claim 29, Holloway et al. teach a spacer formed adjacent the gate structure.

However, An omission of an element and its function if the function of the element is not desired is obvious. See Ex parte Wu , 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989).

With respect to claim 30, Holloway et al. fail to teach the range for the thickness of gate oxide layer.

However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of gate oxide layer through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 31 and 32, Holloway et al. fail to teach the ranges for the concentration of the source, drain, and channel.

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However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to determine the workable or optimal value or range for the concentration of the source, drain, and channel through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that they are critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

6. Claims 34, 35, 36, 37, 38, 39, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway et al. (US patent 4,845,047) as applied to claim 33 above, and further in view of Ueno et al. (US patent 6,815,295).

With respect to claim 34, Holloway et al. fail to teach that the channel is doped by a halo implantation.

However, doping channel by halo implantation is well-known in the art.

With respect to claim 35, Holloway et al. fail to teach that the gate length is in the range between .05 to .25 micrometer.

However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to reduce the length of gate because it is known that shorter gate length would achieve device scaling.

With respect to claim 36, Holloway et al. fail to teach gate oxide comprises of a first oxide layer and a second oxide layer.

Ueno et al. teach a process in which a gate oxide comprises of a first oxide layer and a second oxide layer. See col. 28, lines 15-25.

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It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to form gate oxide made from a first oxide layer and a second oxide layer to reduce the processing steps. See col. 28, line 38.

With respect to claim 37, Holloway et al. teach a spacer formed adjacent the gate structure.

However, An omission of an element and its function if the function of the element is not desired is obvious. See Ex parte Wu , 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989).

With respect to claim 38, Holloway et al. fail to teach the range for the thickness of gate oxide layer.

However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of gate oxide layer through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 39 and 40, Holloway et al. fail to teach the ranges for the concentration of the source, drain, and channel.

However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to determine the workable or optimal value or range for the concentration of the source, drain, and channel through routine experimentation and optimization to obtain optimal or desired device performance because it is a result-effective variable and there is no evidence indicating that they are critical or produces any unexpected results and it has been held that it is not

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inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xong Xham

Primary Examiner

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